

FIG. 1A

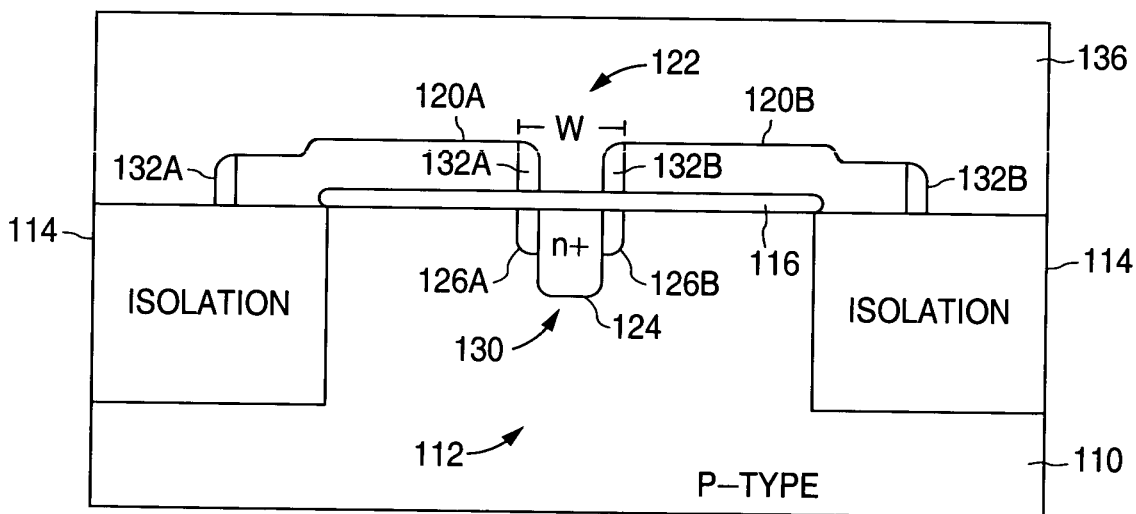


FIG. 1B

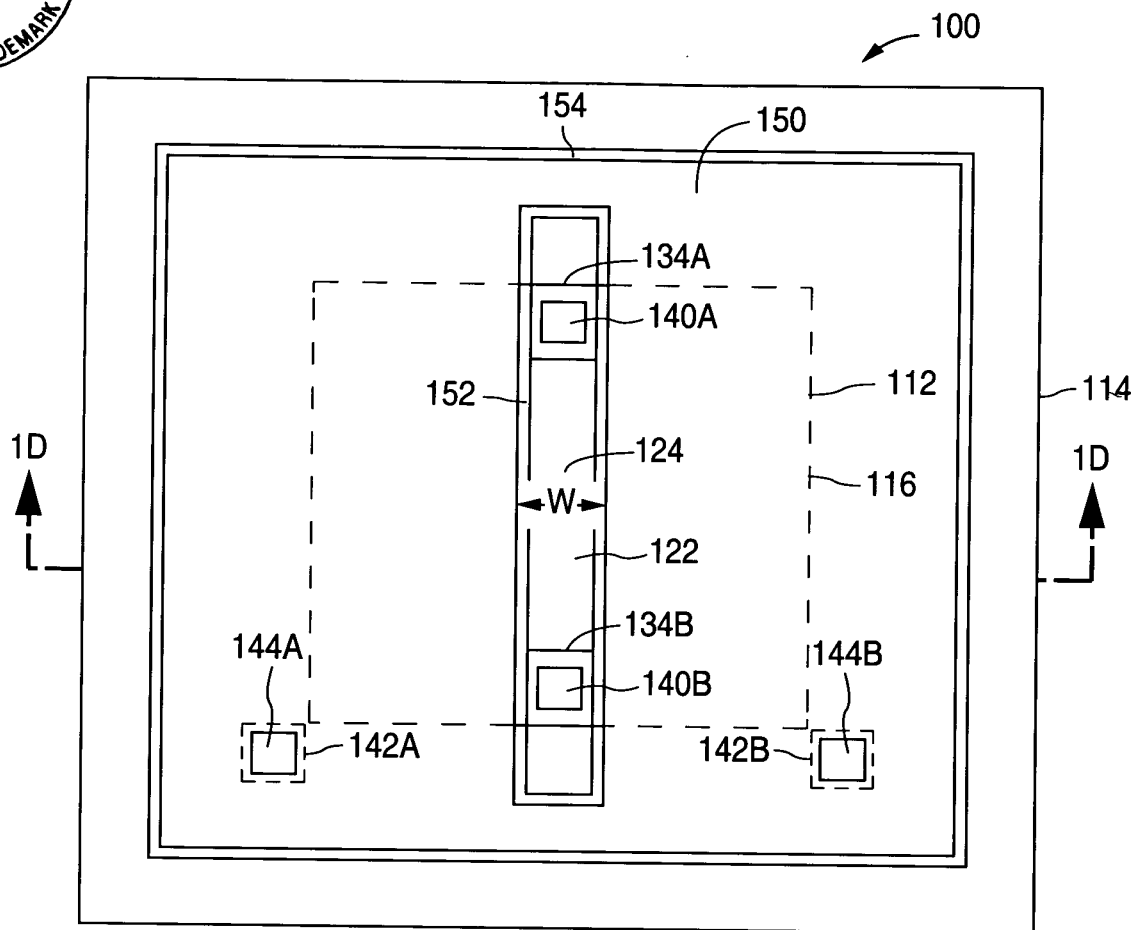


FIG. 1C

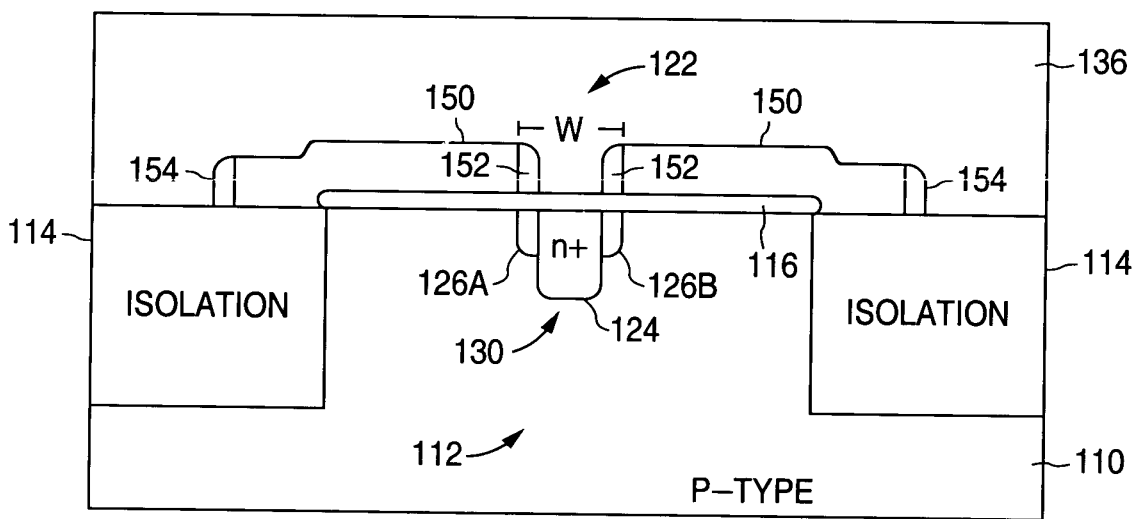
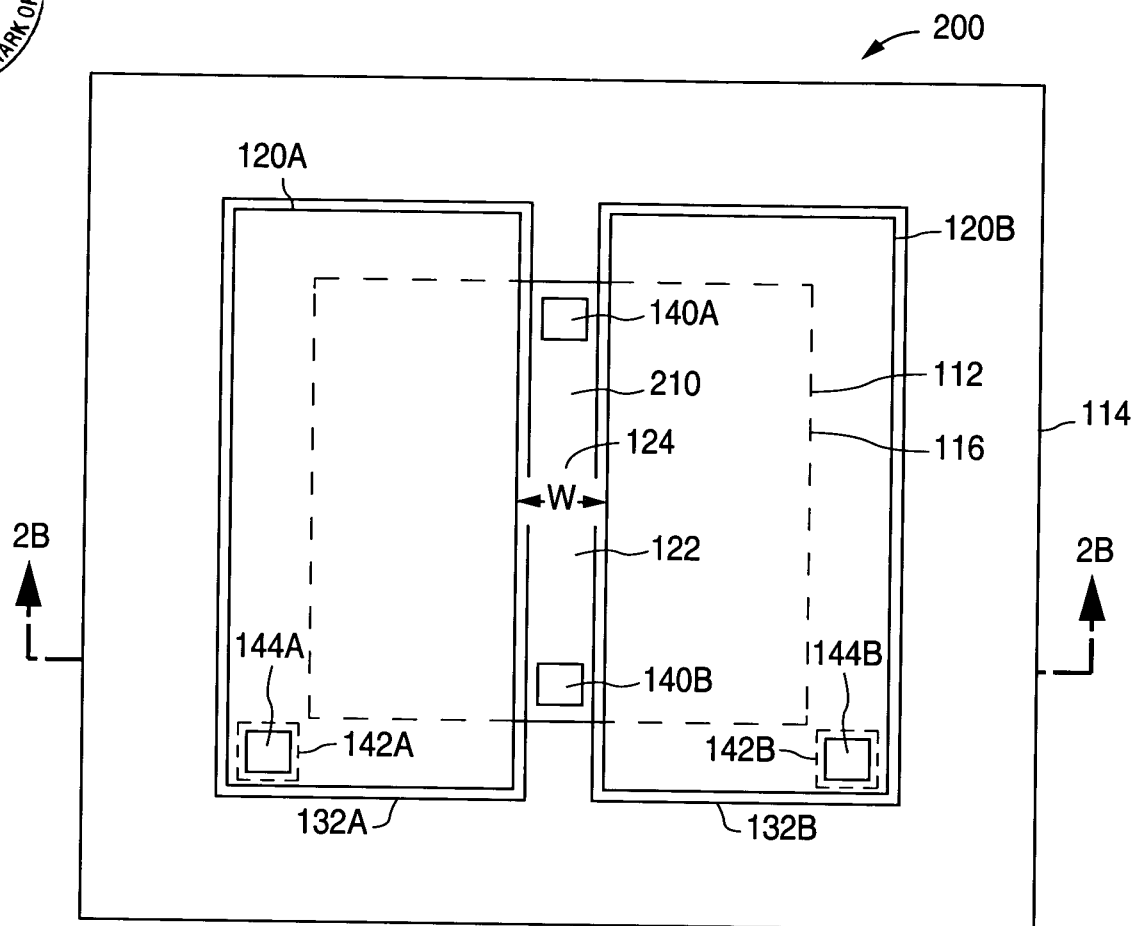


FIG. 1D



This cross-sectional view shows a semiconductor device on a P-TYPE substrate 110. A central n+ region 124 is formed in the substrate, with a vertical contact 140B extending through a dielectric layer 136 to its top surface. The n+ region 124 is flanked by two isolation regions 114. The top surface of the n+ region 124 is covered by a layer 126, which is divided into two parts, 126A and 126B, by a vertical line 120. The top surface of the device is covered by a layer 132, which is divided into two parts, 132A and 132B, by a vertical line 120. The top surface of the device is also covered by a layer 116. The bottom surface of the device is covered by a layer 112. The top surface of the device is also covered by a layer 136.

FIG. 2B

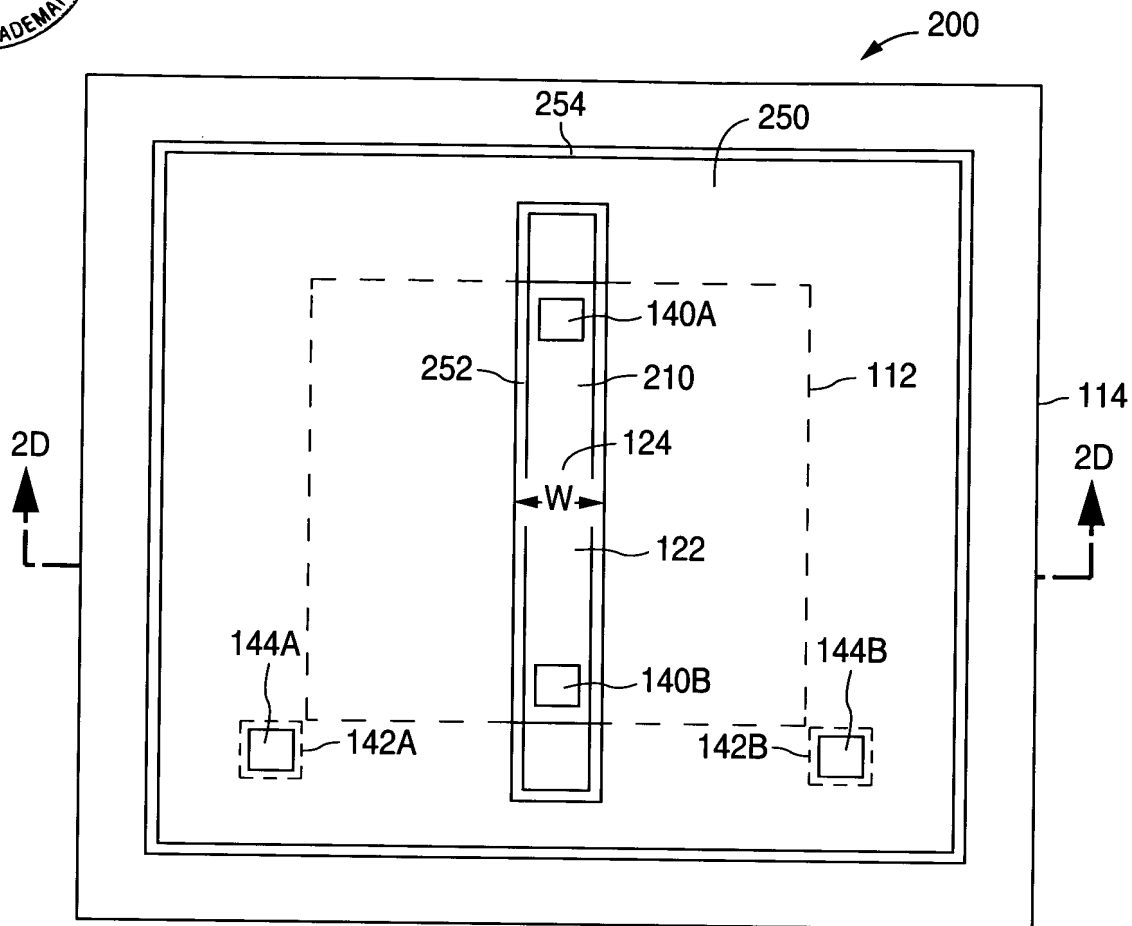


FIG. 2C

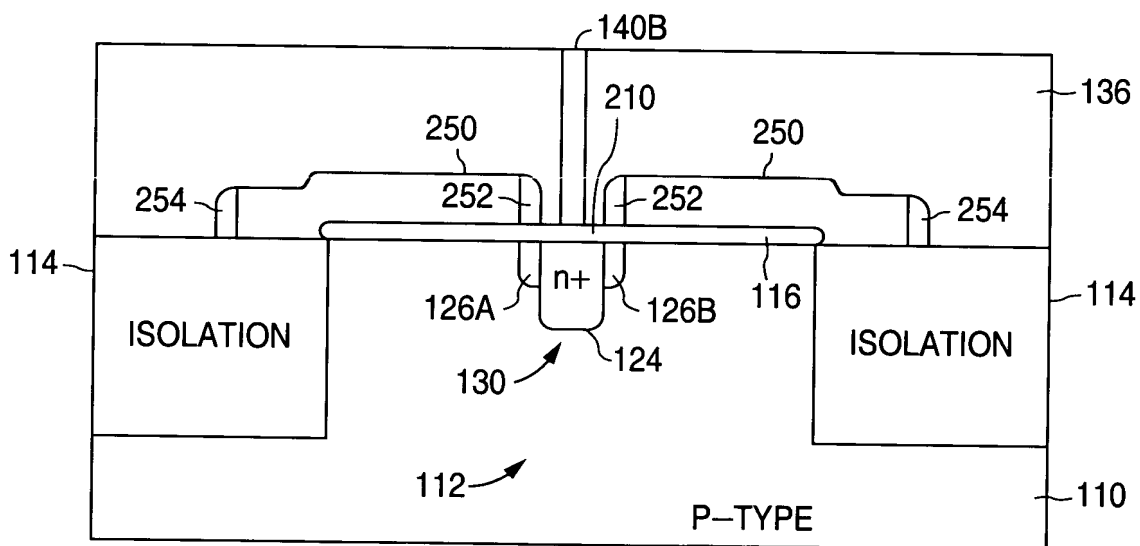


FIG. 2D

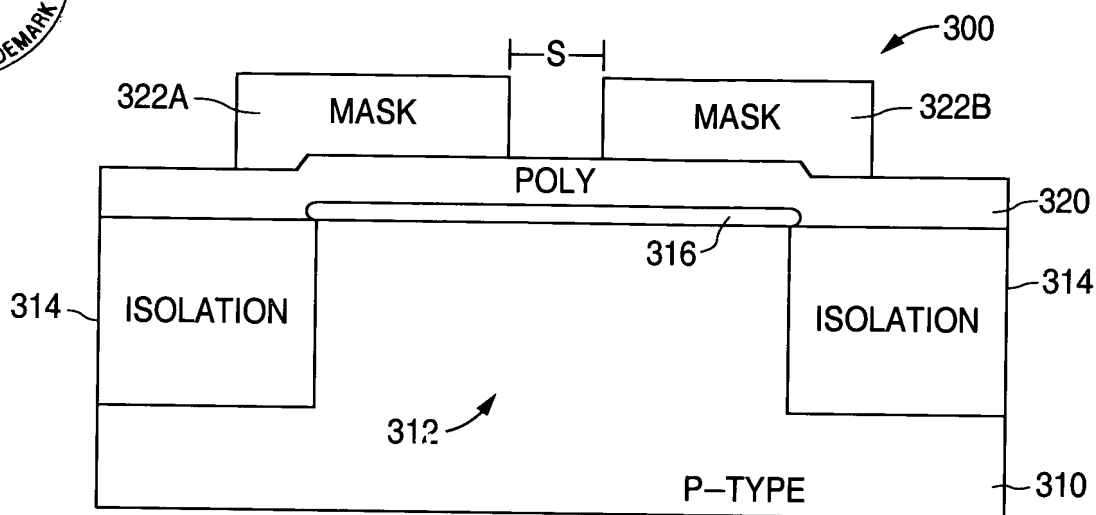


FIG. 3A

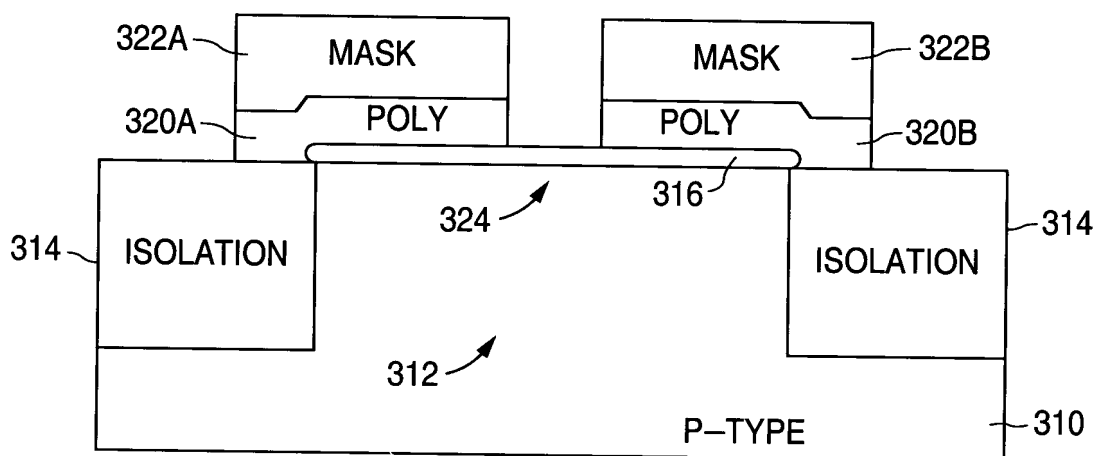


FIG. 3B

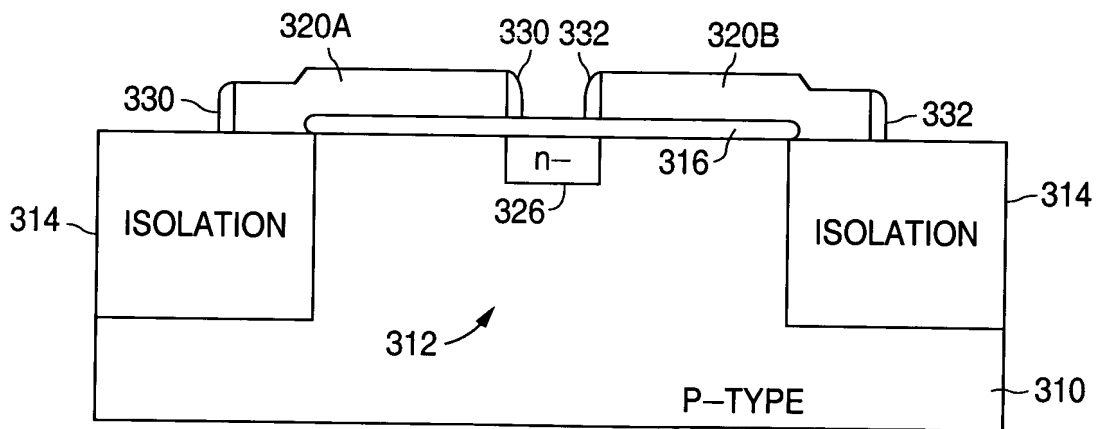


FIG. 3C

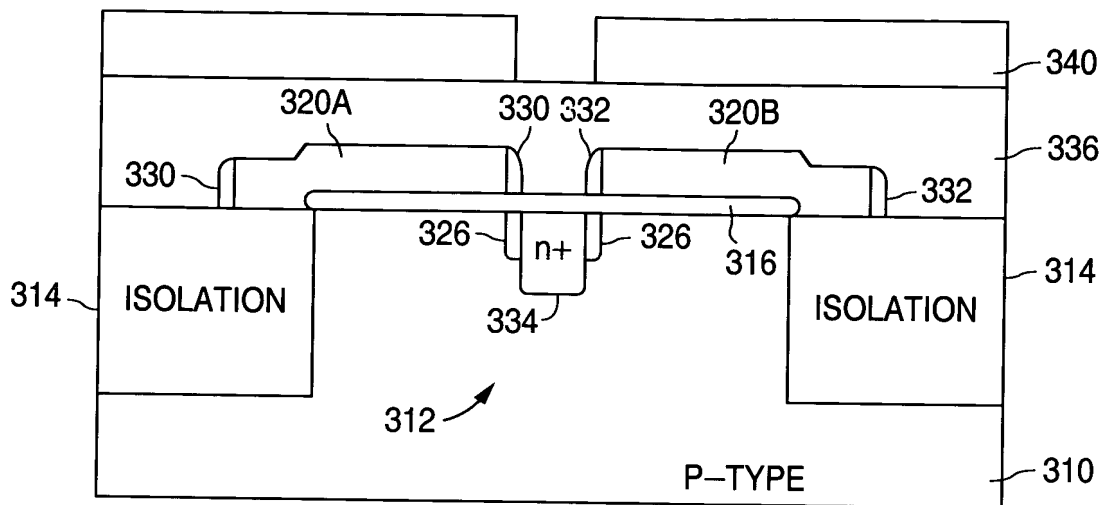


FIG. 3D

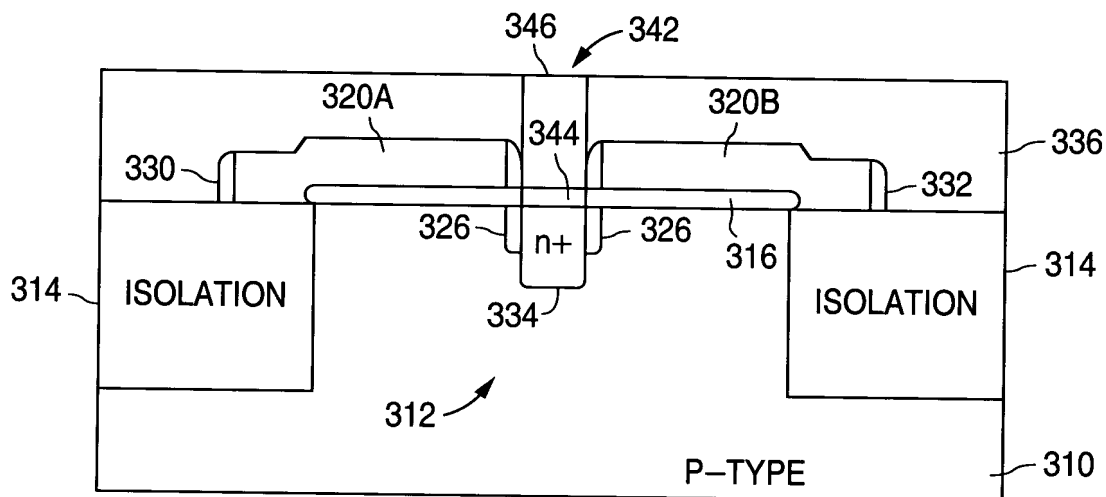


FIG. 3E

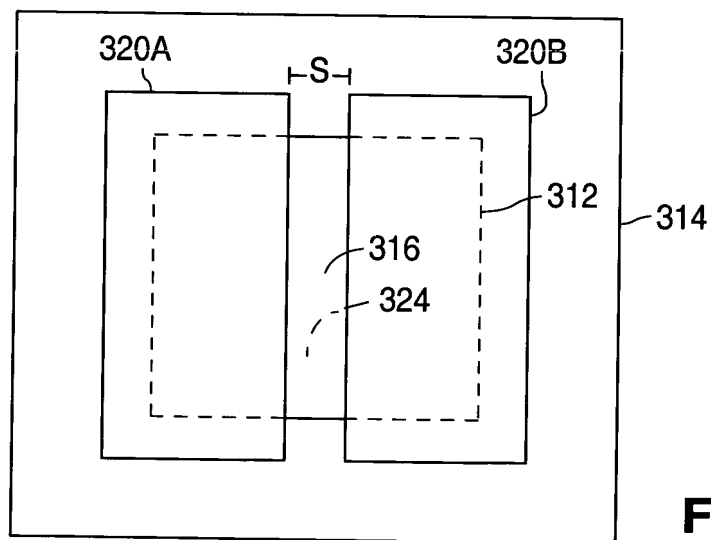


FIG. 4

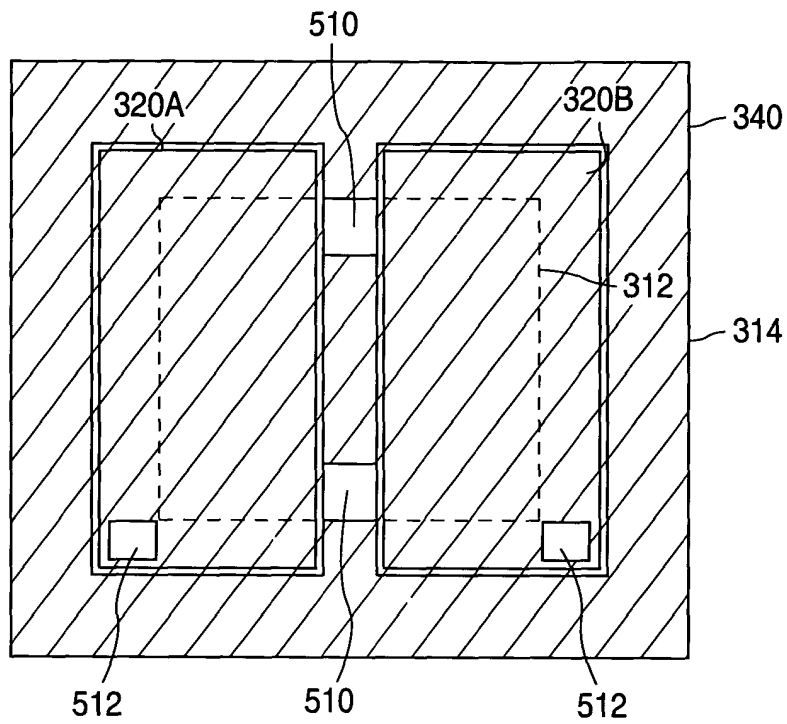


FIG. 5

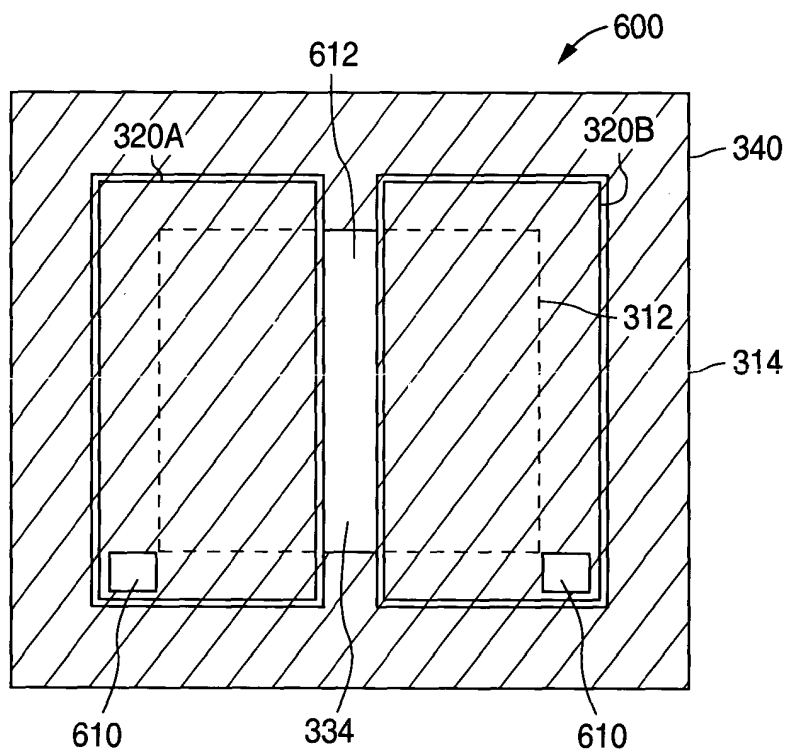


FIG. 6